Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**OUT**

**OUT**

**GND**

**.076”**

**.071”**

**08**

**MASK REF**

**CASE IS INPUT**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .010” X .008”**

**Backside Potential:**

**Mask Ref: 08**

**APPROVED BY: DK DIE SIZE .071” X .076” DATE: 7/25/22**

**MFG: ON SEMI THICKNESS .014” P/N: MCC7908C**

**DG 10.1.2**

#### Rev B, 7/19/02